ABSTRACT

As shown in figure 1, a gate terminal of a MOS transistor or an input terminal of a logic gate, which are included in a through current detection target net list, are extracted, and a resistor is inserted between the gate terminal of the MOS transistor or the input terminal of the logic gate and a power supply, and between the gate terminal of the MOS transistor or the input terminal of the logic gate and a reference voltage, respectively, thereby to perform net list conversion, and thereafter, DC analysis is executed. Therefore, a MOS transistor in which through current might occur can be detected, leading to reliable detection of through current that cannot be easily detected by the conventional DC analysis simulation, and reliable detection of a transistor in which through current might occur, in the through current detection target circuit.